Mitigating Optical Probing at Circuit and Layout Levels: From Design Strategies to Silicon Results

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Abstract

In recent years, a novel non-invasive, laser-assisted Side-Channel Analysis (SCA) technique, namely Optical Probing (OP), has proven effective for probing the internal state of transistors through backside access. Prior works have shown that OP can successfully extract chips' Intellectual Property (IP). Several countermeasures against OP have been proposed; however, they are either ineffective or prohibitively costly, which discourages design houses from adopting them in standard design flows. In this talk, we present a set of design strategies to mitigate OP attacks using an in-house OP security evaluation framework that is compatible with industry-standard design flows. We then implement these countermeasures in a fabricated chip and evaluate their effectiveness in an experimental setup. Overall, this work provides the first end-to-end development of countermeasures against OP attacks, introducing an OP security evaluation framework that aids designers to make informed decisions between power, area, performance, and security in simulation, followed by validation of the proposed countermeasures in silicon.